REMARKS

Favorable reconsideration of this application, in light of the preceding amendments and the following remarks, is respectfully requested.

Claims 1-27 are pending in this application. Claim 27 is newly added. No claims have been cancelled.

Applicants note with appreciation the indication of allowable subject matter in dependent claims 7-18 and 22 and the indication claim 26 is allowable.

The Applicants note with appreciation the Examiner's acknowledgement that certified copies of all priority documents have been received by the USPTO. Action summary at 12.

The Applicants also respectfully note that the present action does not indicate that the drawings have been accepted by the Examiner. The Applicants respectfully request that the Examiner's next communication include an indication as to the acceptability of the filed drawings or as to any perceived deficiencies so that the Applicants may have a full and fair opportunity to submit appropriate amendments and/or corrections to the drawings.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 23 and 24 stand rejected under 35 U.S.C. § 102(b) as anticipated by Lee et al. (U.S. Patent No. 6,277,722, herein Lee). The Applicants respectfully traverse this rejection for the reasons detailed below.

Independent Claim 23 recites a semiconductor device including "a semiconductor substrate; a gate insulator formed on the semiconductor substrate; and a metal gate pattern formed on the gate insulator." More specifically, the metal gate pattern has a top service and substantially vertical sidewalls and includes a first conductor pattern having a first oxidation rate, a second conductor pattern having a second oxidation rate, and a capping layer. Further,

in the metal gate pattern recited in amended claim 23, "**the first oxidation rate of the first conductor pattern is enhanced relative to the second oxidation rate of the second conductor pattern**." (Emphasis added).

As described with respect to an example embodiment of the present invention, "[w]hen a silicon oxide layer is deposited as the first capping layer 22 on the metal gate pattern 30, the **oxidation of the metal layers** included in the metal gate pattern (e.g., a tungsten or a tungsten nitride layer) **may be reduced**."[1] Further, "[t]he **selective oxidation may reduce the oxidation of the second conductive layer** 16 (e.g., tungsten nitride layer) and the third conductive layer 18 (e.g., tungsten layer) in the metal gate pattern and **may selectively oxidize the surface of the silicon substrate 10 and the first conductive layer 14** (e.g., a polysilicon layer)." [2] Therefore, Applicants respectfully submit that according to an example embodiment of the present invention, an oxidation rate of the first conductive pattern **is enhanced** relative to the second oxidation rate of the second conductive pattern.

Lee describes a method for forming a polymetal gate including forming a capping layer, etching the capping layer to remain only on the sidewalls, heating the polymetal gate to repair damage of the capping layer resulting from the etching process, and then performing a reoxidation process.[3] Lee states "because the damage of the nitride film which remains in the sidewalls of the polymetal gate 20 is recovered through the previous heat treatment, the penetration of the oxidizing gas through the exposed portion of the tungsten film 13 is prevented in the reoxidation process."[4] According to the above-cited language of Lee, and illustrated by the differences shown in Figures 3 and 4 of Lee, the repaired nitride sidewalls

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1 Applicants specification, page 15, paragraph [0048].
2 Applicants specification, page 16, paragraph [0050].
3 Lee, Abstract.
4 Lee, Col. 3, Lines 28-34.

prevent the reoxidation step from having any effect on the gate pattern. In other words, only the gate oxide layer 11 on the sides of the gate pattern is modified during the reoxidation process. Therefore, Applicants respectfully submit that Lee fails to disclose a structure, wherein the oxidation rate of the polysilicon layer 12 **is enhanced** relative to metal layers 13 or 14.

Applicants note that the Examiner on page 7, lines 5-6 merely states that "[t]he process of Lee and the present invention render the same structure, as claimed." However, as argued above and previously argued in the amendment filed July 13, 2005, the nitride capping layer described in Lee prevents the metal gate pattern under the capping layer from being affected during a reoxidation process according to the teachings of Lee. Therefore, Applicants respectfully submit that the structure in Lee is not the same as the structure of claim 23. In particular, Lee fails to disclose, teach, or suggest the metal gate pattern of the semiconductor device of amended claim 23 reciting, *inter alia*, "**the first oxidation rate of the first conductor pattern of the metal gate pattern is enhanced relative to the second oxidation rate of the second conductor pattern**."

Further, even if the Examiner cites Lee as inherently disclosing that a polysilicon layer 12 has a first oxidation rate and the metal layers 13 and 14 have a second oxidation rate, Lee does not disclose, teach, or suggest either explicitly or inherently a structure, wherein the first oxidation rate of a first conductor pattern **is enhanced** relative to an oxidation rate of a second conductor pattern.

Still further, MPEP §2112 VI titled "Examiner Must Provide Rationale or Evidence Tending to Show Inherency" states, "the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency or the result or characteristic." In re Rijckaert, 9 F.3d 1531, 1534; 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

Still further, "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter 1990).

Applicants respectfully note that nowhere in the record has the Examiner provided a basis in fact and/or technical reasoning to reasonably support that the metal gate pattern in Lee is even affected by the reoxidation process in Lee, much less that an oxidation rate of a first conductor pattern is enhanced relative to a second conductor pattern.

The Applicants, therefore, respectfully request that the rejection to Claims 23 and claim 24 depending therefrom under 35 U.S.C. § 102(b) be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-6, 19-20, and 25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Lee in view of Kobayashi et al. (U.S. Patent No. 4,505,028 herein Kobayashi).

Initially, Applicants respectfully note that that the following arguments traversing the above rejection were included in the previous Amendment filed July 13, 2005, and that in response to the arguments below the Examiner simply states "[w]ith respect to independent claims 1-6 and 19-21 (method claims), the reoxidation has nothing to do with the portion of Si that is covered by the nitride layer but the independent claims are directed toward the oxidation of the substrate, Kobayashi describes a wet oxidation process that is well known in the art, Lee discusses the use of a wet oxidation process in forming his structure, therefore it would be obvious that Lee can be completed with a well known wet oxidation process." However, Applicants respectfully submit that the above conclusory statement does not address the following arguments indicating that (1) Lee teaches away from the claimed

invention, (2) that the above-quoted portion does not provide sufficient evidence in the record for modifying the method of forming an integrated circuit of Lee to incorporate the selective oxidation step of Kobayashi, and (3) that incorporating the selective oxidation step of Kobayashi into the method of forming an integrated circuit described in Lee would change the basic principle of the operation of the method described in Lee. These arguments are detailed below.

Claim 1 recites a method for fabricating a semiconductor device having a metal gate pattern including:

> forming a gate insulating layer having an initial thickness on a silicon substrate;
>
> depositing a metal gate material on the gate insulating layer, the metal gate material including at least one metal layer;
>
> etching the metal gate material to form a metal gate pattern;
>
> forming a capping layer on the metal gate pattern; and
>
> selectively oxidizing at least a portion of the silicon substrate without substantially oxidizing the at least one metal layer and **without substantially increasing the initial thickness of the gate insulating layer**." (Emphasis added).

As illustrated by the comparison of the conventional devices illustrated in Figures 2A and 2B with the semiconductor devices developed according to the method of claim 1 shown in Figures 12A and 12B, the selectively oxidizing step of claim 1 oxidizes the at one metal layer "**without substantially increasing the initial thickness of the gate insulating layer**."[5] As shown in the non-limiting example of Figure 12B, the gate oxide layer is only increased from a thickness of 55 Å to 63 Å, whereas the conventional oxidation processes increase the gate oxide layer from 55 Å to 90 Å, approximately doubling the thickness of the gate oxide layer.

The outstanding Office Action on page 5, lines 10-16, acknowledges that Lee fails to disclose "selectively oxidizing at least a portion of the silicon substrate without substantially

oxidizing the at least one metal layer and without substantially increasing the initial thickness of the gate insulating layer" and relies on the teachings of Kobayashi for this feature of claim 1.

In addition to the above-identified deficiency of Lee, Applicants respectfully submit that Lee teaches away from the method recited in claim 1. More specifically, Lee states "the technique using the capping layer has a disadvantage in that the exposed portion of the tungsten is oxidized as usual in the following reoxidation in spite of the formation of the nitride film for oxidation prevention."[6] In other words, Lee states that forming sidewalls (capping layer) without heating the sidewalls prior to oxidization has no effect since the sidewalls are damaged and the oxidizing gas will penetrate the damaged sidewalls causing adverse effects. Accordingly, Applicants respectfully submit that an essential feature of the method of Lee is the heating process completed after the forming of the sidewalls and prior to the oxidization of the substrate. Therefore, Applicants respectfully submit that Lee teaches away from the method of the claimed invention.

With respect to the proposed combination of Lee and Kobayashi, Applicants respectfully submit that the combination is improper for at least the following reasons.

Lee is directed to preventing migration of the oxidizing gases through the nitride sidewalls, which must be repaired during a heating process, whereas the teachings of Kobayashi describe that selective oxidation may be used to oxidize "silicon alone without substantially oxidizing tungsten, molybdenum or their silicides."[7] Therefore, according to the teachings of Kobayashi, there is no need for the sidewalls or repairing the sidewalls since silicon can be selectively etched without effecting metals such as tungsten. Accordingly,

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5 Applicants' specification at least at page 23, paragraph [0071].

6 Lee, column 2, lines 3-6.

Applicants respectfully submit there is insufficient evidence in the record for modifying the method of forming an integrated circuit of Lee to incorporate the selective oxidation step of Kobayashi. Additionally, neither Lee nor Kobayashi recognize the problems or solution thereto regarding the increase in thickness of a gate insulating layer within the metal gate pattern.

Further, Applicants respectfully submit that an attempt to bring in the isolated teachings of the selective oxidation step of Kobayashi into the method for forming an integrated circuit of Lee would amount to improperly picking and choosing from the different references without regard for the teachings of the references as a whole.[8] In addition, Applicants respectfully submit that incorporating the selective oxidation step of Kobayashi into the method of forming an integrated circuit described in Lee would change the basic principle of the operation of the method described in Lee, which is to prevent oxidation of the metal gate by creating sidewalls and heating the sidewalls to repair damage incurred during the formation of the sidewalls.

Still further, Applicants respectfully submit that even if one skilled in the art is motivated to combine the references of Lee and Kobayashi, the result of the combination would likely be the elimination of Lee's sidewalls (i.e. the capping layer). Therefore, the combination of Lee and Kobayashi would still not teach or suggest the features of claim 1.

The Applicants maintain, therefore, that the Action does not present the required "convincing line of reasoning as to why the artisan would have found the claimed invention

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[7] Kobayashi, column 2, lines 35-37.

[8] See In re Ehrreich 590 F2d 902, 200 USPQ 504 (CCPA, 1979) (stating that patentability must be addressed "in terms of what would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the sum of all the relevant teachings in the art, not in view of first one and then another of the isolated teachings in the art," and that one "must consider the entirety of the disclosure made by the references, and avoid combining them indiscriminately.")

to have been obvious in light of the teachings of the references," *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985), and that this rejection may not be properly maintained absent such reasoning.

Claims 2-6, 19, and 20 depend from claim 1 and claim 25 recites features similar to claim 1. Therefore, the arguments discussed above regarding the deficiencies of Lee with respect to independent claim 1 and the improper combination of Lee and Kobayashi also apply to claims 2-6, 19, 20, and 25.

Accordingly, Applicants respectfully request that the rejection to claims 1-6, 19, and 20 and 25 under 35 U.S.C. § 103(a) be withdrawn.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Lee in view of Kobayashi, and further in view of Hwang et al. (U.S. Patent No. 6,245,605, herein Hwang). The Applicants respectfully traverse this rejection for the reasons detailed below.

The Applicants respectfully incorporate the discussion above with respect to the deficiencies of both Lee and Kobayashi and with respect to the lack of motivation to make the proposed combination of method steps suggested by the Examiner.

Further, Applicants respectfully submit that Hwang, like Kobayashi, utilizes selective oxidation to avoid the need to form the protective sidewalls of Lee during the reoxidation process and, therefore, would not provide one of ordinary skill in the art with the requisite motivation to make the proposed combination for the reasons discussed above in connection with Kobayashi. Further, the Applicants respectfully contend that even were such a combination to be made, the teachings of Hwang are not sufficient to remedy the noted deficiencies in Lee and Kobayshi.

Accordingly, Applicants respectfully request that the rejection of claim 21 under 35 U.S.C. § 103 be withdrawn.

ALLOWABLE SUBJECT MATTER

The Applicants note with appreciation the Examiner's indication that claims 7-18 and 22 are objected to as being dependent from a rejected based claim, and would, therefore, be allowable if rewritten in independent form incorporating limitations of all included claims. As reflected by the remarks above, however, the Applicants respectfully maintain that the remaining claims are also allowable for at least the same reasons as independent claim 1 and that no such rewriting of claims 7-18 and 22 is warranted at this time.

NEW CLAIMS

Claim 27 has been added in an effort to provide further protection for the Applicants' invention. Claim 27 depends from independent claim 23 and recites that the "capping layer is a silicon oxide layer." Claim 27 is believed to be in condition for formal allowance.

CONCLUSION

In view of the above remarks and amendments, the Applicants respectfully submit that each of the pending objections and rejections have been addressed and overcome, leaving the present application for condition for formal allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

If necessary, the Commissioner is hereby authorized and in this, concurrent, and future replies, to charge any under payment or non-payment of any fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, or credit any overpayment of such fees, to Deposit Account No. 08-0750, including, in particular, extension of time fees.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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